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Digital Electronics MCQ

Digital Electronics Test

DIGITAL ELECTRONICS OBJECTIVE QUESTIONS- PHASE 1

1.In which of the following base systems is 123 not a valid number?
(a) Base 10
(b) Base 16
(c)Base8
(d) Base 3

Ans:d

2. Storage of 1 KB means the following number of bytes
(a) 1000
(b)964
(c)1024
(d) 1064.

Ans:d
3. What is the octal equivalent of the binary number:
10111101
(a)675
(b)275
(c) 572
(d) 573.
Ans:b

4. Pick out the CORRECT statement:
(a) In a positional number system, each symbol represents the same value irrespective of its position
(b) The highest symbol in a position number system as a value equal to the number of symbols in the system
(c) It is not always possible to find the exact binary
(d) Each hexadecimal digit can be represented as a sequence of three binary symbols.
Ans:c

5.The binary code of $(21.125)_{10}$ is
(a) 10101.001
(b) 10100.001
(c) 10101.010
(d) 10100.111.

Ans:a
6.A NAND gate is called a universal logic element because
(a) it is used by everybody
(b) any logic function can be realized by NAND gates alone

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(c) all the minization techniques are applicable for optimum NAND gate realization
(d) many digital computers use NAND gates.
Ans:b

7. Digital computers are more widely used as compared to analog computers, because they are
(a) less expensive
(b) always more accurate and faster
(c) useful over wider ranges of problem types
(d) easier to maintain.
Ans:c

8. Most of the digital computers do not have floating point hardware because
(a) floating point hardware is costly
(b) it is slower than software
(c) it is not possible to perform floating point addition by hardware
(d) of no specific reason.
Ans:a

9. The number 1000 would appear just immediately after
(a) FFFF (hex)
(b) 1111 (binary)
(c) 7777 (octal)
(d) All of the above.
Ans:d

10. $(1(10101)_2$ is
(a) $(37)_{10}$
(b) $(69)_{10}$
(c) $(41)_{10}$
(d) — $(5)_{10}$
Ans:a

11. The number of Boolean functions that can be generated by n variables is equal to
(a) 2^n
(b) $2^{2\ n}$
(c) 2^{n-1}
(d) — 2^n

Ans:b

12. Consider the representation of six-bit numbers by two's complement, one's complement, or by sign and magnitude: In which representation is there overflow from the addition of the integers 011000 and 011000?
(a) Two's complement only
(b) Sign and magnitude and one's complement only

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(c) Two's complement and one's complement only
(d) All three representations.
Ans:d

13. A hexadecimal odometer displays F 52 F. The next reading will be
(a)F52E
(b)G52F
(c)F53F
(d)F53O.
Ans:d

14. Positive logic in a logic circuit is one in which
(a) logic 0 and 1 are represented by 0 and positive voltage respectively
(b) logic 0 and, -1 are represented by negative and positive voltages respectively
(c) logic 0 voltage level is higher than logic 1 voltage level
(d) logic 0 voltage level is lower than logic 1 voltage level.
Ans:d

15. Which of the following gate is a two-level logic gate
(a) OR gate
(b) NAND gate
(c) EXCLUSIVE OR gate
(d) NOT gate.
Ans:c

16. Among the logic families, the family which can be used at very high frequency greater than 100 MHz in a 4 bit
synchronous counter is
(a) TTLAS
(b) CMOS
(c)ECL
(d)TTLLS
Ans:c

17. An AND gate will function as OR if
(a) all the inputs to the gates are "1"
(b) all the inputs are '0'
(c) either of the inputs is "1"
(d) all the inputs and outputs are complemented.
Ans:d

18. An OR gate has 6 inputs. The number of input words in its truth table are
(a)6
(b)32
(c) 64

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(d) 128
Ans:c

19. A debouncing circuit is
(a) an astable MV
(b) a bistable MV
(c) a latch
(d) a monostable MV.
Ans:c

20. NAND. gates are preferred over others because these
(a) have lower fabrication area
(b) can be used to make any gate
(c) consume least electronic power
(d) provide maximum density in a chip.
Ans:b

21. In case of OR gate, no matter what the number of inputs, a
(a) 1 at any input causes the output to be at logic 1
(b) 1 at any input causes the output to be at logic 0
(c) 0 any input causes the output to be at logic 0
(d) 0 at any input causes the output to be at logic 1.
Ans:a

22. The fan put of a 7400 NAND gate is
(a)2TTL
(b)5TTL
(c)8TTL
(d)10TTL
Ans:d

23. Excess-3 code is known as
(a) Weighted code
(b) Cyclic redundancy code
(c) Self-complementing code
(d) Algebraic code.

Ans:c

24. Assuming 8 bits for data, 1 bit for parity, I start bit and 2 stop bits, the number of characters that 1200 BPS communication line can transmit is
(a)10 CPS
(b)120 CPS
(c) 12CPS
(d) None of the above.
Ans:c

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25. Indicate which of the following three binary additions are correct?
1.1011 + 1010 = 10101
II. 1010 + 1101 = 10111
III. 1010 + 1101 = 11111
(a) I and II
(b) II and III
(c) III only
(d) II and III

Ans:d

PHASE-2

DIGITAL ELECTRONICS OBJECTIVE QUESTIONS -PART-1

1.The number of digits in octal system is
a.8
b.7
c.10
d. none

2..The number of digits in Hexadecimal system is
a.15
b.17
c.16
d. 8

3.The number of bits in a nibble is
a.16
b.5
c.4
d.8

4.The digit F in Hexadecimal system is equivalent to —— in decimal system
a.16
b.15

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c.17
d. 8

5.Which of the following binary numbers is equivalent to decimal 10
a.1000
b.1100
c.1010
d.1001

6.The number FF in Hexadecimal system is equivalent to —— in decimal system
a.256
b.255
c.240
d.239

7.IC s are
a. analog
b. digital
c. both analog and digital
d. mostly analog

8.The rate of change of digital signals between High and Low Level is
a. very fast
b. fast
c. slow
d. very slow

9. Digital circuits mostly use
a. Diodes
b. Bipolar transistors
c. Diode and Bipolar transistors
d. Bipolar transistors and FETs

10.Logic pulser
a. generates short duration pulses
b. generate long duration pulses
c. generates long and short duration
d. none of above

11.What is the output state of an OR gate if the inputs are 0 and 1?
a.0
b.1
c.3
d.2

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12.What is the output state of an AND gate if the inputs are 0 and 1?
a.0
b.1
c.3
d.2

13.A NOT gate has…
a. Two inputs and one output
b. One input and one output
c. One input and two outputs
d. none of above

14.An OR gate has…
a. Two inputs and one output
b. One input and one output
c. One input and two outputs
d. none of above

15.The output of a logic gate can be one of two _____?
a. Inputs
b. Gates
c.States
d. none

16.Logic states can only be ___ or 0.
a. 3
b. 2
c.1
d.0

17.The output of a ____ gate is only 1 when all of its inputs are 1
a. NOR
b. XOR
c. AND
d. NOT

18.A NAND gate is equivalent to an AND gate plus a …. gate put together.
a. NOR
b. NOT
c. XOR
d. none

19.Half adder circuit is ______?
a. Half of an AND gate
b. A circuit to add two bits together

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c. Half of a NAND gate
d. none of above

20. Numbers are stored and transmitted inside a computer in
a. binary form
b. ASCII code form
c. decimal form
d. alphanumeric form

21.The decimal number 127 may be represented by
a. 1111 1111B
b. 1000 0000B
c. EEH
d. 0111 1111

22.. A byte corresponds to
a. 4 bits
b. 8 bits
c. 16 bits
d. 32 bits

23.A gigabyte represents
a.1 billion bytes
b. 1000 kilobytes
c. 230 bytes
d. 1024 bytes

24. A megabyte represents
a. 1 million bytes
b. 1000 kilobytes
c. 220 bytes
d. 1024 bytes

25.. A Kb corresponds to
a. 1024 bits
b. 1000 bytes
c.210 bytes
d. 210 bits

<u>Answers of DIGITAL ELECTRONIC MULTIPLE CHOICE QUESTIONS-1</u>

1. a
2.c
3.c
4.b

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5.c
6.b
7.c
8.a
9.c
10.b
11. b
12.a
13. b
14. a
15. a
16. c
17.c
18. b
19.b
20.a
21. d
22. b
23. a
24. a
25.b

DIGITAL ELECTRONICS MULTIPLE CHOICE QUESTIONS-2 | Indian Shout

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DIGITAL ELECTRONICS MULTIPLE CHOICE QUESTIONS-2

DIGITAL ELECTRONICS OBJECTIVE QUESTIONS -PART-2

26.A parity bit is
a. used to indicate uppercase letters
b. used to detect errors
c. is the first bit in a byte
d. is the last bit in a byte

27. Which of these devices are two state.
a. lamp
b. punched card
c. magnetic tape
d. all the above

28.The output impedance of of a logic pulser is
a. low
b. high
c. may be low or high
d. none of above

28.The number of LED display indicators in logic probe are
a.1
b.2
c.1 or 2
d.4

29.In hexadecimal number system,A is equal to decimal number
a.10
b.11
c.17
d.18

30.Hexadecimal number F is equal to octal number
a.15
b.16
c.17
d.18

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31.Hexadecimal number E is equal to binary number
a.1110
b.1101
c.1001
d.1111

32.Binary number 1101 is equal to octal number
a.15
b.16
c.17
d.14

33.Octal number 12 is equal to decimal number
a.8
b.11
c.9
d. none

34.Decimal number 10 is equal to binary number
a.1110
b.1000
c.1001
d.1010

35.Binary number 110011011001 is equal to decimal number
a.3289
b.2289
c.1289
d.289

36.1111+11111=
a.101111
b.101110
c.111111
d.011111

37.Binary multiplication 1*0=
a.1
b.0
c.10
d.11

38.110012 -100012=
a.10000
b.01000

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c.00100
d.00001

39.10112*1012=
a.55
b.45
c.35
d.25

40.1110112*100012=
a.111101101
b.111101100
c.111110
d.1100110

41.4 bits is equal to
a. 1 nibble
b.1 byte
c. 2 byte
d. none of above

42. which is non-volatile memory
a. RAM
b. ROM
c. both
d. none

43. The contents of these chips are lost when the computer is switched off?
a. ROM chips
b. RAM chips
c. DRAM chips
d. none of above

44.What are responsible for storing permanent data and instructions.?
a. RAM chips
b. ROM chips
c. DRAM chips
d. none of above

45. Which parts of the computer perform arithmetic calculations?
a. ALU
b. Registers
c. Logic bus
d. none of above

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46.How many bits of information can each memory cell in a computer chip hold?
a. 0 bits
b. 1 bit
c. 8 bits
d. 2 bits

47.What type of computer chips are said to be volatile?
a. RAM chips
b. ROM chips
c. DRAM
d. none of above

48.Which generation of computer uses more than one microprocessor?
a. Second generation
b. Fifth generation
c.Third generation
d .none of above

49.Which generation of computer developed using integrated circuits?
a. Second generation
b. Fifth generation
c. Third generation
d. none of above

50.Which generation of computer was developed from microchips?
a. Second generation
b. Third generation
c. Fourth generation
d. none of above

“DIGITAL ELECTRONICS MULTIPLE CHOICE QUESTIONS-2”

1. *Anoop* says:

   March 27, 2012 at 5:13 pm

   26. b
   27. a
   29. a
   30.c
   31. a
   32. a
   33. d
   34.d

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35. a
36. b
37. b
38. a
41. a
42. a
43. b
44. b
45. a
46. b
47. a
48. c
49. a
50. b

Please send the correct answers of Digital electronics Multiple choice- 2

DIGITAL ELECTRONICS OBJECTIVE QUESTIONS-3 | Indian Shout

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DIGITAL ELECTRONICS OBJECTIVE QUESTIONS-3

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DIGITAL ELECTRONICS MULTIPLE CHOICE QUESTIONS -PART-3

51.RAM can be expanded to a
a. increase word size
b. increase word number
c. increase word size or increase word number
d. none of above

52. Which memory is available in all technologies
a. PROM
b. EEPROM
c. ROM
d. EPROM

53. Which memory does not require programming equipment
a. PROM
b. EEPROM
c. ROM
d. EPROM

54. In CCD
a. small charge is deposited for logical 1
b. small charge is deposited for logical 0 or 1
c. small charge is deposited for logical 0 and large charge for logical 1
d. none of above

55. The internal structure of PLA is similar to
a. RAM
b. ROM
c. both RAM or ROM
d. neither RAM nor RAM

56.An output of combinational ckt depends on
a. present inputs
b. previous inputs
c. both present and previous
d .none of above

57.Which are combinational gates
a. NAND & NOR
b. NOT & AND
c. X-OR & X-NOR
d. none of above

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58.. As access time is decreased, the cost of memory
a. remains the same
b. increases
c. decreases
d. may increase or decrease

59. Which is correct:
a. A.A=0
b. A+1=A
c. A+A=A’
d. A’.A’=0

60.A counter is a
a. Sequential ckt
b. Combinational ckt
c. both combinational and sequential ckt
d. none of above

61.The parity bit is
a. always 1
b. always 0
c.1 or 0
d.none of above

62.In 2 out of 5 code,decimal number 8 is
a.11000
b.10100
c.1100
d.1010

63.In number of information bits is 11,the number of parity Bits in hamming code is
a.5
b.4
c.3
d.2

64.For a 4096*8 EPROM ,the number of address lines is
a.14
b.12
c.10
d.8

65. 23.6 10=……….2
a.11111.10011
b.10111.10011

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c.00111.101
d.10111.1

66.BCD number 0110011=…….10
a.66
b.67
c.68
d.69

67.The total number of input states for 4 input or gate is
a.20
b.16
c.12
d.8

68.In a 4 input OR gate,the total number of High outputs for the 16 input states are
a.16
b.15
c.13
d. none of above

69.In a 4 input AND gate,the total number of High outputs for the 16 input states are
a.16
b.8
c.4
d.1

70.a buffer is
a. always non-inverting
b.always inverting
c. inverting or non-inverting
d.none of above

71.An AND gate has two inputs A and B and ine inhibits input S.Output is 1 if
a.A=1,B=1,S=1
b. A=1,B=1,S=0
c. A=1,B=0,S=1
d. A=1,B=0,S=0

72. An AND gate has two inputs A and B and ine inhibits input S.Out of total 8 input states,Output is 1 in
a. 1 states
b. 2 states
c. 3 states
d. 4 states

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73.In a 3 input NOR gate,the number of states in which output is 1 equals
a. 1
b. 2
c. 3
d. 4

74.Which of these are universal gates
a. only NOR
b. only NAND
c. both NOR and NAND
d. NOT,AND,OR

75. In a 3 input NAND gate,the number of gates in which output in 1equals
a.8
b.7
c.6
d..5

76. A XOR gate has inputs A and B and output Y.Then the output equation is
a.Y=A+B
b.Y=AB+A'B
c.AB+ AB'
d.AB'+A'B'

77.A 14 pin NOT gate IC has……….NOT gates
a.8
b.6
c.5
d.4

78.A 14 pin AND gate IC has……….AND gates
a.8
b.6
c.4
d.2

79.The first contribution to logic was made by
a. George Boole
b. Copernicus
c. Aristotle
d. Shannon

80.Boolean Alzebra obeys
a. commutative law
b. associative law

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c. distributive law
d. commutative, associative, distributive law

81. A+(B.C)=
a. A.B+C
b. A.B+A.C
c. A
d.(A+B).(A+C)

82.A.0=
a. 1
b. A
c. 0
d. A or 1

83.A+A.B=
a. B
b. A.B
c. A
d. A or B

84.Demorgan's first theorem is
a. A.A'=0
b. A''=A
c. (A+B)'=A'.B'
d. (AB)'=A'+B'
85. Demorgan's second theorem is
a. A.A'=0
b. A''=A
c. (A+B)'=A'.B'
d. (AB)'=A'+B'

86. Which of the following is true
a. SOP is a two level logic
b. POS is a two level logic
c. both SOP and POS are two level logic
d. Hybrid function is two level logic

87.The problem of logic race occurs in
a. SOP functions
b. Hybrod functions
c. POS functions
d. SOP and POS functions

88. In which function is each term known as min term
a. SOP

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b. POS
c. Hybrid
d. both SOP and POS

89. In which function is each term known as max term
a. SOP
b. POS
c. Hybrid
d. both SOP and Hybrid

90. In the expression A+BC, the total number of min terms will be
a.2
b. 3
c.4
d. 5

91.The min term designation for ABCD is
a.m0
b. m10
c. m14
d. m15

92. The function Y=AC+BD+EF is
a. POS
b. SOP
c. Hybrid
d. none of above

93. The expression Y=∏M(0,1,3,4) is
a. POS
b. SOP
c. Hybrid
d. none of above

94. AB+AB'=
a. B
b. A
c.1
d. 0

95. In a four variable Karnaugh map eight adjacent cells give a
a. Two variable term
b. single variable term
c. Three variable term
d. four variable term

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96.A karnaugh map with 4 variables has
a. 2 cells
b. 4 cells
c. 8 cells
d.16 cells

97.In a karnaugh map for an expression having 'don't care terms' the don't cares can be treated as
a. 0
b. 1
c. 1 or 0
d. none of above

98. The term VLSI generally refers to a digital IC having
a. more than 1000 gates
b. more than 100 gates
c. more than 1000 but less than 9999 gates
d. more than 100 but less than 999 gates

99.Typical size of an IC is about
a.1"*1"
b. 2"*2"
c. 0.1"*0.1"
d. 0.0001"*0.0001"

100.A digital clock uses…………..chip
a. SSI
b. LSI
c. VLSI

answers of above questions which i think .
53-c
56-c
57-b
58-b
64-b
67-b
68-b
69-d
71-a
72-a
73-a
74-c
75-b

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76-Y=AB’=A’B
77-d
78-c
79-a
81-b
82-c
84-c
85-d
88-a
89-b
90-a
91-d
92-b
93-a
94-b
95-b
96-d
97-c

DIGITAL ELECTRONICS OBJECTIVE QUESTIONS-4 | Indian Shout

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DIGITAL ELECTRONICS OBJECTIVE QUESTIONS-4

DIGITAL ELECTRONICS MULTIPLE CHOICE QUESTIONS-PART-4

101. Digital technologies being used now-a-days are
a. DTL and EMOS
b. TTL, ECL, CMOS and RTL
c. TTL, ECL and CMOS
d. TTL, ECL, CMOS and DTL

102. A TTL circuit with totem pole output has
a. high output impedance
b. low output impedance
c. very high output impedance
d. any of above

103. TTL uses
a. multi emitter transistors
b. multi collector transistors
c. multi base transistors
d. multi emitter or collector transistors

104. Advanced schottky is a part of
a. ECL family
b. CMOS family
c. TTL family
d. none of above

105. For wired AND connection we should use
a. TTL gates with active pull up
b. TTL gates with open collector
c. TTL gates without active pull up and with open collector
d. any of above

106. Time delay of a TTL family is about
a. 180ns
b. 50ns
c. 18ns
d. 3 ns

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107. As compared to TTL, ECL has
a. lower power dissipation
b. lower propagation delay
c. higher propagation delay
d. higher noise margin

108. As compared to TTL, CMOS logic has
a. higher speed of operation
b. higher power dissipation
c. smaller physical size
d. all of above

109. 74HCT00 series is
a.NAND IC
b. interface between TTL and CMOS
c. inverting IC
d. NOR IC

110.CD 4010 is a
a. inverting buffer
b. non inverting hex buffer
c. NOR IC
d. NAND IC

111. Current requirement of a piezo buffer is about
a. 100mA
b. 20mA
c. 4 mA
d. 0.4 mA

112. TSL inverter has
a. one input
b. two inputs
c. one or two inputs
d. three inputs

113. Parallel adder is
a. sequential circuits
b. combinational circuits
c. either sequential or combinational circuits
d. none of above

114. The inputs to a 3 bit binary adder are 1112 and 1102. The output will be
a.101
b.1101

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c.1111
d.1110

115. A half adder can be used only for adding
a. 1s
b. 2s
c. 4s
d. 8s

116. A 3 bit binary adder should be
a. 3 full adders
b. 2 full adders and 1 half adder
c. 1 full adder and 2 half adder
d. 3 half adders

117. when two 4 bit parallel adders are cascaded we get
a. 4 bit parallel adder
b. 8 bit parallel adder
c. 16 bit parallel adder
d. none of above

118. The widely used binary multiplication method is
a. repeated addition
b. add and shift
c. shift and add
d. any of above

119.When microprocessor processes both positive and negative numbers, the representation used is
a. 1's complement
b. 2's complement
c. signed binary
d. any of above

120. Decimal -90 =…………in 8 bit 2s complement
a.1000 1000
b.1010 0110
c.1100 1100
d.0101 0101

121. In 2's complement addition, the carry generated in the last stage is
a. added to LSB
b. neglected
c. added to bit next to MSB
d. added to the bit next to LSB

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122. The number of inputs and outputs in a full adder are
a. 2 and 1
b. 2 and 2
c. 3 and 3
d. 3 and 2

123.In a 7 segment display the segments a,c,d,f,g are lit. The decimal number displayed will be
a. 9
b. 5
c. 4
d. 2

124. In a 7 segment display the segments b and c are lit up. The decimal number displayed will be
a. 9
b. 7
c. 3
d. 1

125 .A device which converts BCD to seven segments is called
a. encoder
b. decoder
c. multiplexer
d. none of these

126. Which device use the nematic fluid
a. LED
b. LCD
c. VF display
d. none of these

127. Which of these is the most recent device
a. LED
b. LCD
c. VF display
d. a and c

128. VF glows with ………. Colour when activated
a. red
b. orange
c. bluish green
d. none of these

129. Which display device resembles vacuum tube
a. LED

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b. LCD
c. VF
d. none of these

130.Which device changes parallel data to serial data
a. decoder
b. multiplexer
c. demultiplexer
d. flip flop

131.A 1 of 4 multiplexer requires…… data select line
a. 1
b. 2
c. 3
d. 4

132. It is desired to route data from many registers to one register. The device needed is
a. decoder
b. multiplexer
c. demultiplexer
d. counter

133.Which device has one input and many outputs
a. flip flop
b. multiplexer
c. demultiplexer
d. counter

134.Two 16:1 and one 2:1 multiplexers can be connected to form a
a. 16:1 multiplexer
b. 32:1 multiplexer
c. 64:1 multiplexer
d. 8:1 multiplexer

135. A flip flop is a
a. combinational circuit
b. memory element
c. arithmetic element
d. memory or arithmetic

136. I n a D latch
a. data bit D is fed to S input and D' to R input
b. data bit D is fed to R input and D' to S input
c. data bit D is fed to both R and S inputs
d. data bit D' is not fed to any input

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137. I n a D latch
a. a high D sets the latch and low D resets it
b. a low D sets the latch and high D resets it
c. race can occur
d. none of above

138.In a positive edge triggered JK flip flop
a. High J and High K produce inactive state
b. Low J and High K produce inactive state
c. High J and Low K produce inactive state
d. Low J and Low K produce inactive state

139.In a positive edge triggered D flip flop
a. D input is called direct set
b.Preset is called direct reset
c. present and clear are called direct set and reset respectively
d. D input overrides other inputs

140. In a positive edge triggered JK flip flop
J=1,K=0 and clock pulse is rising.Q will
a. be 0
b. be 1
c. show no change
d. toggle

141. For edge triggering in flip flops manufacturers use
a. RC circuit
b. direct coupled design
c. either RC circuit or direct coupled design
d. none of these

142. In a JK flip flop toggle means
a. set Q=1 and Q'=0
b. set Q=0 and Q'=1
c. change the output to the opposite state
d. no change in input

143. A mod 4 counter will count
a. from 0 to 4
b. from 0 to 3
c. from any number n to n+4
d. none of above

144.A counter has N flip flops. The total number of states are
a. N
b. 2N

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c. 2N
d. 4N

145.A counter has modulus of 10. The number of flip flops are
a. 10
b. 5
c. 4
d. 3

146.In a ripple counter
a. whenever a flip flop sets to 1,the next higher FF toggles
b. whenever a flip flop sets to 0,the next higher FF remains unchanged
c. whenever a flip flop sets to 1,the next higher FF faces race condition
d. whenever a flip flop sets to 0,the next higher FF faces race cond

147.A counter has 4 flip flops.It divides the input frequency by
a.4
b. 2
c. 8
d. 16

148. A decade counter skips
a. binary states 1000 to 1111
b. binary states 0000 to 0011
c. binary states 1010 to 1111
d. binary states 1111 and higher

149.The number of flip flops needed for Mod 7 counter are
a. 7
b. 5
c. 3
d. 1

150.A presettable counter with 4 flip flops start counting from
a. 0000
b. 1000
c. any number from 0000 to 1111
d. any number from 0000 to 1000
151.A 4 bit down counter can count from
a. 0000 to 1111
b. 1111 to 0000
c. 000 to 111
d. 111 to 000

152. A 3 bit up-down counter can count from
a. 000 to 111

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b. 111 to 000
c. 000 to 111 and also from 111 to 000
d. none of above

153.IC counters are
a. synchronous only
b. asynchronous only
c. both synchronous and asynchronous
d. none of above

154. Shifting digits from left to right and vice versa is needed in
a. storing numbers
b. arithmetic operations
c. counting
d. storing and counting

155. The basic storage element in a digital system is
a. flip flop
b. counter
c. multiplexer
d. encoder

156. The simplest register is
a. buffer register
b. shift register
c. controlled buffer register
d. bidirectional register

157. The basic shift register operations are
a. serial in serial out
b. serial in parallel out
c. parallel in serial out
d. all of above

158. A universal shift register can shift
a. from right to left b. from left to right
c. both from right to left and left to right
d. none of above

159. In a shift register, shifting a bit by one bit means
a. division by 2
b. multiplication by 2
c. subtraction by 2
d. any of above

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160. An 8 bit binary number is to be entered into an 8 bit serial shift register. The number of clock pulses required is
a. 1
b. 2
c. 4
d. 8